

Listing of the Claims

1. (Currently Amended) A field-effect transistor, comprising:
~~having a doped channel region arranged along a first depression,~~
~~having a doped first terminal region near an opening of the first~~
depression,
~~having a doped second terminal region remote from the opening, the~~
~~second terminal comprising a connecting region extending up from a portion of the~~
~~second terminal region approximately as far as a surface containing the opening or~~
~~being electrically conductively connected to an electrically conductive connection~~
~~leading to the surface,~~
~~having a control region arranged in the first depression,~~
~~and ~~having~~ an electrical insulating region between the control region and~~
the channel region, and
~~a second depression between the first terminal region and the connecting~~
~~region,~~
~~the terminal region remote from the opening leading as far as a surface~~
~~containing the opening or being electrically conductively connected to an electrically~~
~~conductive connection leading to the surface, the field-effect transistor being a drive~~
transistor at a word line or at a bit line of a memory cell array, the field-effect transistor
comprising only one depression in which the control region is arranged.
2. (Currently Amended) The field-effect transistor as claimed in claim 1,
wherein the first and second terminal regions comprise substantially ~~contain~~ the same
dopant concentration and dopants of the same conduction type.
3. (Currently Amended) The field-effect transistor as claimed in claim 1
wherein the channel region ~~has~~ comprises a length corresponding to at least two thirds
of a depth of the first depression.

4. (Currently Amended) The field-effect transistor as claimed in claim 1, wherein the first depression is a trench or a hole.

5. (Currently Amended) The field-effect transistor as claimed in claim 4, wherein the channel region lies on opposing sides of the trench ~~or along an entire periphery of the hole~~.

6. (Currently Amended) The field-effect transistor as claimed in claim 4, wherein the channel region lies ~~only on one side of the trench or only along part of a~~ periphery of the hole.

7. (Cancelled)

8. (Currently Amended) The field-effect transistor as claimed in claim 1, wherein the first depression for the control region and a third depression filled with an electrical insulating material between the field-effect transistor and an adjacent electrical component have the same depth.

9. (Currently Amended) The field-effect transistor as claimed in claim 1, wherein the first depression for the control region has a smaller depth than a third depression filled with an electrical insulating material between the field-effect transistor and an adjacent electronic component.

10. (Currently Amended) The field-effect transistor as claimed in claim 1, wherein the electrical insulating region has an insulating thickness of at least 15 nm.

11-12. (Cancelled)

13. (Withdrawn) A method comprising:
fabricating a field-effect transistor having the following steps to be performed without restriction by the order specified:

provision of a carrier material having a surface to be processed,
formation of a terminal region near the surface and a terminal
region remote from the surface,

formation of at least one depression, which leads from the terminal
region near the surface as far as the terminal region remote from the surface or which
leads from a region for the terminal region near the surface to a region for the terminal
region remote from the surface, the field effect transistor comprising only one
depression in which a control region is arranged,

production of an electrical insulating layer in the depression,
introduction of an electrically conductive control region into the
depression; and

using the field-effect transistor at a word line or a bit line of a memory cell
array.

14. (Withdrawn) The methods as claimed in claim 13, wherein the formation of
the terminal regions is performed at least one of: before the formation of the depression
and before filling of the depression.

15. (Withdrawn) The method as claimed in claim 13, comprising the following
step: formation of a connecting region from the terminal region remote from the surface
to a surface of a semiconductor layer.

16. (Withdrawn) The method as claimed in claim 13, wherein at least one
insulating depression is formed at the same time as the depression for the control
region.

17. (Withdrawn) The method as claimed in claim 16, wherein the insulating
depression is formed with the same depth as the depression for the control region.

18. (Withdrawn) The method as claimed in claim 16, wherein the insulating
depression is made deeper than the depression for the control region.

19. (Withdrawn) The method as claimed in claim 18, wherein the insulating depression is wider than the depression for the control region at least in an upper section, and wherein the two depressions are formed in a common etching process in which wider depressions are etched more deeply than narrower depressions.

20. (Currently Amended) The field-effect transistor as claimed in claim 1, further comprising wherein at least one of:
a distance between the first and second terminal regions along the first depression is at least 0.4 μm , and
~~at least one terminal region has a shallow doping profile gradient which permits a switching voltage having a magnitude of greater than 9 volts but less than 30 volts.~~

21. (Withdrawn) A method of using a field-effect transistor having a doped channel region arranged along a depression, a doped terminal region near an opening of the depression, a doped terminal region remote from the opening, a control region arranged in the depression, and an electrical insulating region between the control region and the channel region, the terminal region remote from the opening leading as far as a surface containing the opening or being electrically conductively connected to an electrically conductive connection leading to the surface, and comprising only one depression in which the control region is arranged, the method comprising: using the field-effect transistor as a driving transistor at a word line or a bit line of a flash memory of an EEPROM memory module.

22. (Withdrawn) A method of using a field-effect transistor having a doped channel region arranged along a depression, a doped terminal region near an opening of the depression, a doped terminal region remote from the opening, a control region arranged in the depression, and an electrical insulating region between the control region and the channel region, the terminal region remote from the opening leading as far as a surface containing the opening or being electrically conductively connected to

an electrically conductive connection leading to the surface, and comprising only one depression in which the control region is arranged, the method comprising: using the field-effect transistor for switching a voltage having a magnitude of greater than 9 volts but less than 30 volts.

23. (New) The field-effect transistor as claimed in claim 1, wherein at least one terminal region has a shallow doping profile gradient which permits a switching voltage having a magnitude of greater than 9 volts but less than 30 volts.

24. (New) The field-effect transistor as claimed in claim 1, wherein the first depression comprises a width of approximately 150 nm.

25. (New) The field-effect transistor as claimed in claim 1, wherein a width of the first depression is approximately equal to a width of the second depression.

26. (New) The field-effect transistor as claimed in claim 1, wherein the first depression comprises a depth of approximately 1 μm .

27. (New) The field-effect transistor as claimed in claim 1, wherein the first and second terminal regions each comprise a top side and a bottom side, wherein the bottom side of the first terminal region faces the top side of the second terminal region, and wherein a distance between the top side of the first terminal region and a middle portion of the second terminal region is approximately 1 μm .

28. (New) The field-effect transistor as claimed in claim 1, wherein the first depression extends from the opening to approximately half-way through the second terminal region.